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Computer Organization & Architecture SOLUTION INTR is a signal which if enabled then microprocessor has interrupt enabled it receives high INR signal & activates INTA signal, so another request can't be accepted till CPU is busy in servicing interrupt. Hence (A) is correct option.
Question. 12

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B. Parhami, Computer Arithmetic: Algorithms and Hardware Designs, 2nd edition, Oxford University Press, New York, 2010. (ISBN 978-0-19-532848-6, 641+xxv pp., 316 figures, 718 problems)
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Behrooz Parhami - Electrical and Computer Engineering

Computer Architecture. Spring 2004 David Brooks. Assistant Professor. Maxwell Dworkin 141 33 Oxford Street Cambridge MA 02138 Phone: 617-495-3989 Fax: 617-495-2809 E-mail: dbrooks@eecs.harvard.edu. Syllabus. Meeting time. Monday/Wednesday 1:00-2:30PM, MD G135. Related Course . CS 246: Advanced Computer Architecture

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